Agència
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Memòria justificativa de recerca de les convocatòries BCC, BE, BP, CTP-AIRE, DEBEQ, FI, INEFC, NANOS i PIV

La memòria justificativa consta de les dues parts que venen a continuació:
1.- Dades bàsiques i resums
2.- Memòria del treball (informe científic)

Tots els camps són obligatoris

1.- Dades bàsiques i resums

Nom de la convocatòria

BE

Llegenda per a les convocatòries:

BCC	Convocatòria de beques per a joves membres de comunitats catalanes a l'exterior
BE	Beques per a estades per a la recerca fora de Catalunya
BP	Convocatòria d'ajuts postdoctorals dins del programa Beatriu de Pinós
CTP-AIRE	Ajuts per accions de cooperació en el marc de la comunitat de treball dels Pirineus. Ajuts de mobilitat de personal investigador.
DEBEQ (Modalitat A3)	Beques de Cooperació Internacional i Desenvolupament
FI	Beques predoctorals per a la formació de personal investigador
INEFC	Beques predoctorals i de col·laboració, dins de l'àmbit de l'educació física i l'esport i les ciències aplicades a l'esport
NANOS	Beques de recerca per a la formació en el camp de les nanotecnologies
PIV	Beques de recerca per a professors i investigadors visitants a Catalunya

Títol del projecte: ha de sintetitzar la temàtica científica del vostre document.
Simulations of parasitic and intrinsic capacitances related to Multiple-Gate-Field-Effect Transistor architectures

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Paraules clau: cal que esmenteu cinc conceptes que defineixin el contingut de la vostra memòria.
Cutoff frequency, FinFET, Fringing capacitance, DG MOSFET, Volume Inversion

Data de presentació de la justificació
24.07.2008

Nom i cognoms i signatura
del/de la investigador/a

Visttiplau del/de la responsable de la
sol·licitud

Resum del projecte: cal adjuntar dos resums del document, l'un en anglès i l'altre en la llengua del document, on s'esmenti la durada de l'acció

Resum en la llengua del projecte (màxim 300 paraules)
El treball que he realitzat a la Université Catholique de Louvain té dues parts. A la primera part, l'impacte d'importants paràmetres geomètrics, com el gruix de font i drenador, espaiat dels "fins", amplada dels "spacers", etc, al component de capacitat paràsita de fricció en les transistors MOSFETs de porta múltiple ("multiple-gate MOSFETs") es va analitzar a fons usant simulacions d'elements finits. Vàries arquitectures, com els "single-gate", FinFETs, "double-gate", "triple-gate" representat pel "Pi-gate MOSFET" es varen simular i comparar en termes de les capacitats de canal i fricció per la mateixa àrea ocupada a l'oblea. Les simulacions destacaren el gran impacte de disminuir l'espaiat entre els multiple-gate MOSFEts i el balanç entre la reducció de les resistències paràsites de font i drenador, i l'increment de les capacitats de fricció quan s'introdueix el creixement selectiu epitaxial ("Selective Epitaxial Growth", SEG). També es va discutir l'impacte d'aquestes solucions tecnològiques a les freqüències de tall del transistor.

La segona part va tractar de l'estudi de l'efecte de la inversió volúmica a les capacitats dels MOSFETs de doble porta (DG MOSFETs) no dopats. Amb aquest objectiu, hem presentat resultats de simulació per a les capacitats de DG MOSFETs no dopats utilitzant un model compacte, analític i explicit. Es va demostrar que es va simular bé la transició des del règim d'inversió volúmica al comportament de porta dual. El model mostra una dependència acurada en el gruix de la capa de silici, consistent amb simulacions numèriques bidimensionals, per silici tant gruixut com prim. Mentre que la conducció de corrent i la transconductància s'incrementen en el règim d'inversió volúmica, els nostres resultats mostren que les capacitats intrínseques presenten valors més alts també, que poden limitar el comportament d'alta velocitat (temps de retard) dels DG MOSFETs sota la inversió volúmica

Resum en anglès (màxim 300 paraules)
My work developed at the Université Catholique de Louvain has two parts.
In the first part, the impact of important geometrical parameters such as source and drain thickness, fin spacing, spacer width, etc. on the parasitic fringing capacitance component of multiple-gate field-effect transistors (MuGFET) is deeply analyzed using finite element simulations. Several architectures such as single gate, FinFETs (double gate), triple-gate represented by Pi-gate MOSFETs are simulated and compared in terms of channel and fringing capacitances for the same occupied die area. Simulations highlight the great impact of diminishing the spacing between fins for MuGFETs and the trade-off between the reduction of parasitic source and drain resistances and the increase of fringing capacitances when Selective Epitaxial Growth (SEG) technology is introduced. The impact of these technological solutions on the transistor cut-off frequencies is also discussed.
The second part deals with the study of the effect of the volume inversion (VI) on the capacitances of undoped Double-Gate (DG) MOSFETs. For that purpose, we present simulation results for the capacitances of undoped DG MOSFETs using an explicit and analytical compact model. It demonstrates that the transition from volume inversion regime to dual gate behaviour is well simulated. The model shows an accurate dependence on the silicon layer thickness,consistent with two dimensional numerical simulations, for both thin and thick silicon

Resum en anglès (màxim 300 paraules) – continuació -.
films. Whereas the current drive and transconductance are enhanced in volume inversion regime, our results show that intrinsic capacitances present higher values as well, which may limit the high speed (delay time) behaviour of DG MOSFETs under volume inversion regime.

2.- Memòria del treball (informe científic sense limitació de paraules). Pot incloure altres fitxers de qualsevol mena, no més grans de 10 MB cadascun d'ells.

Simulations of parasitic capacitances related to Multiple-Gate-Field-Effect Transistor architectures

In order to pursue the scaling of MOS devices into the 45-nm technology node, nonplanar double-gate (FinFETs) and triple-gate MOSFETs (Pi-gate FETs) have become attractive for their good control of short channel effects and high current drive [1]. Currently, the technological trend points towards the FinFET device as a likely-to-emerge structure also thanks to its excellent compatibility with the quasi-planar Si technology [2]. However, large series resistances, which are induced by the narrow-fin nature of nonplanar MOSFETs, result in a significant degradation of current drive in direct current operation regions. In order to retain the advantages of a narrow fin width without compromising the drive current or transconductance, techniques like SEG are employed [3]. The SEG technology is effective in decreasing the parasitic S/D resistance, which translates into improved drive current. The impact of SEG dimensions on the parasitic MuGFET capacitances will be discussed in our work. A recent FinFET geometrical approach has been proposed in [4], observing the capacitance parasitics, but without considering SEG technology impact. One of the primary requirements for MuGFETs to be a technology enabler is that they must have at least the same current drive as the planar technology, for identical layout area [5]. So, in order to find out which are the dimensions for an optimum MuGFET, we compare the parasitic and channel capacitances between the different analyzed MOSFETs, based on equal die area occupation. In this way, we develop new design guidelines for the best performance.
Furthermore, to thoroughly investigate the influence of geometrical parameters on the RF performance, we present the simulated cutoff frequencies of MuGFETs with respect to the fins spacing and to the introduction of SEG.

I. CAPACITANCE ANALYSIS

COMSOL software uses the proven finite-element analysis (FEA) method to efficiently model any physical phenomena which can be described by partial differential equations. Due to its tight coupling into MATLAB, the simulations can be done very fast and easy compared to other commercially available simulation tools. For the simulation of a single gate transistor (SG) we consider a very wide fin, with thick gate oxide on both sides of that fin; and for the Pi-gate transistor simulation we consider an extension of the gate into the buried oxide (BOX) and a thin top gate oxide (triple gate). In order to

consider the most up to date geometrical parameters for MuGFETs, we intensively reviewed the recent publications [1-12] on that topic. Table 1 summarizes the main geometrical parameters considered in this work for the nominal SG and MuGFETs, considering the same occupied area. The capacitance values have been normalized to the actual occupied planar silicon die area:

$$A = W_{tot} \cdot L_g \quad (1)$$

where W_{tot} is the total occupied silicon width of the transistor and L_g, the gate length (Table 1).
The total occupied silicon width for MuGFETs is:

$$W_{tot} = (N_{fin} - 1)(S_{fin} + W_{fin} + 2 \cdot t_{ox}) + (W_{fin} + 2 \cdot t_{ox}) = 4280\,nm \quad (2)$$

where N_{fin}, S_{fin}, W_{fin} and t_{ox} are, respectively, the number of fins, the fins spacing, the fin width and the gate oxide.
For the nominal SG transistor, the transistor width to occupy the same area is the total occupied silicon width of MuGFET reduced by twice the side oxide (Table 1):

$$4280 - 2 \cdot 30 = 4220\,nm$$

As it will be explained later on, the optimization of the $C_{channel}/C_{fringing}$ ratio is of first importance to improve the analog/RF performance of MOSFETs. For the nominal dimensions summarized in Table 1, we obtain a very good agreement between the simulated values of this ratio and the measurements presented in [6].
In the following sections, we simulate the impact of the main geometrical parameters (spacer width, S_{fin}, SEG, gate extension depth for Pi-gate) on the fringing and channel capacitances, in strong inversion. These capacitances are calculated by integration of the surface charge in the fin region, for the channel capacitance (theoretical intrinsic capacitance), and outside the channel for the fringing capacitance - mainly between the vertical poly-Si gate and the fin, but also through the BOX.

MuGFET		**SG**	
Fin Width (W_{fin})	20	Transistor Width	4220
Fin Height	60	Silicon Thickness	60
PolySi gate	100	PolySi gate	100
Gate oxide (t_{ox})	2	Gate oxide (t_{ox})	2
No. of fins (N_{fin})	20	-	-
SEG thickness	30	SEG thickness	30
Gate length	50	Gate length	50
Hardmask	30	Side Oxide	30
Spacer Width	40	Spacer Width	40
BOX thickness	150	BOX thickness	150
S_{fin}	200	-	-
$C_{channel}$ (F/m^2)	0.009	$C_{channel}$ (F/m^2)	0.017
$C_{fringing}$ (F/m^2)	0.005	$C_{fringing}$ (F/m^2)	0.005
$C_{channel}/C_{fringing}$	1.8	$C_{channel}/C_{fringing}$	3.4

Table 1. Nominal values for the studied devices. All geometrical dimensions are given in nm.

A. Integration level

From Table 1, we notice that the normalized channel capacitance is higher in the case of the SG, due to a higher effective width for the same occupied Si area, which translates into a higher drive current (when we assume that both devices have the same mobility and the same source-drain resistances), whereas the relative importance of the fringing capacitance is higher for FinFET. Our goal is to have at least the same drive current in a FinFET as in a SG for the same occupied area, so we should increase the fin height or decrease the spacing between fins (pitch). Indeed, multiple-fin devices can exceed the area efficiency of traditional planar devices if the fin height is greater than half the pitch. However, the fin height is somehow technologically limited due to aspect ratio (fin width/fin height) and topography considerations [7]. In fact, increasing the ratio between fin width and fin height causes degradation of the gate control over the active channel for a fixed gate length [8]. Nowadays, the ratio does not exceed 1/6 [4], so the fin height is limited to typically 50 to 100 nm [9]. Also, the increased topography impacts the gate lithography and etching [10] as well as the silicidation process of the contacts. Thus, due to these technological limitations regarding the fin height, as presented in Section C, we analyzed the impact of the fin spacing of MuGFET on the drive current density and also on the parasitic capacitances.

B. Impact of SEG technology

One of the major disadvantages of MuGFETs with narrow fin width is the associated high parasitic S/D resistances, which degrade drive current and transconductance. For its minimization it is desirable to widen the S/D extension regions alone without widening the body region [3], i.e. without compromising short channel control. This is achieved using SEG technology. As presented in [11], a SEG thickness of 50 nm reduces the series resistances by a factor of 4. However, the drawback of the SEG process is an increase in the parasitic capacitance. Hence, there exists a trade-off between series S/D resistance minimization and parasitic capacitance incrementation.

Our simulations are in agreement with the measurements in [3], where they experimentally observed a 10% increase of the parasitic capacitance with the introduction of SEG process. It can be noted that the ratio is lower in the case of the FinFET for the nominal value of the fin spacing found in the literature. It means that the parasitic fringing capacitances are relatively more important in the case of FinFETs compared to SG. As presented in the next Section, the maximization of this ratio, and so, the decrease of the fringing capacitances for MuGFETs can be achieved by reducing the spacing between fins.

C. Impact of fin spacing

First of all, by minimizing the fin spacing we assure a higher drive current for MuGFETs for the same occupied Si area. We show the channel and fringing capacitances for a SG and various FinFETs characterized by different fin spacings and different numbers of fins (the occupied area being fixed). We find that for a fin spacing below 100 nm, the normalized drive current of FinFETs is higher than the one of a SG. The absolute value of the fringing capacitance for FinFETs also increases with the decrease of fin spacing, i.e. with the increasing number of fins, but the relative importance of these fringing capacitances is greatly decreased (higher $C_{channel}/C_{fringing}$ ratio) with the reduction of S_{fin}. Indeed, for a fin spacing of 60 nm the $C_{channel}/C_{fringing}$ ratio of FinFET reaches a similar value as for SG. R. Rooyackers *et al.* [12] obtained a record fin pitch of 50 nm, by a fin doubling and quadrupling technique based on spacer defined fin patterning.

D. Impact of gate extension depth into the BOX

In [8], J.-P. Colinge showed that Pi-gate structure – extension of gate material into the BOX - could be of great interest for controlling short channel effects in MuGFETs. We indeed notice a nice increase of the channel capacitance for Pi-gate devices compared to FinFET architecture. But our simulations also show that the fringing capacitance increases with the extension depth for values higher than 10 nm. The optimum $C_{channel}/C_{fringing}$ ratio (higher channel capacitance and lower fringing capacitance) for Pi-gate is obtained for a gate extension of 10 nm - $C_{channel}/C_{fringing}$ = 2.2 (compared to 1.9 for FinFET).

E. Impact of spacer width

For minimizing the source and drain resistances, the spacer width can be optimized, without modifying the channel control, to values lower than 20 nm [11]. Unfortunately, a decrease of the spacer width will lead to an increase of the fringing capacitances, therefore, we face again a trade-off.

II. CUTOFF FREQUENCIES

In previous section, we have shown the impact of SEG and fin spacing on the fringing capacitances. As we mentioned, using SEG technology there is a tradeoff between the reduction of series resistances and the increase of fringing capacitances. Based on the expressions (3) and (4) the current gain and maximum available gain cutoff frequencies, respectively, have been calculated using the equivalent lumped elements extracted from measurements in [6] and the $C_{channel}/C_{fringing}$ (C_{gs}/C_{gd}) ratio simulated in this work.

$$f_T = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+(R_s+R_d)\left(\frac{C_{gd}}{C_{gs}}(g_m+g_d)+g_d\right)} \tag{3}$$

with $f_c = \frac{g_m}{2\pi C_{gs}}$

$$f_{max} = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)} \frac{1}{2\cdot\sqrt{g_d(R_g+R_s+R_i)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left((R_s+R_i)g_m+\frac{C_{gd}}{C_{gs}}\right)}} \tag{4}$$

It is demonstrated clearly the existence of an optimum SEG thickness layer, which achieves the best trade-off between the series resistances (R_s and R_d) and the C_{gd}/C_{gs} ratio, corresponding to the peak

values of f_t and f_{max}. We observe an improvement of both cutoff frequencies with the reduction of S_{fin}, thanks to the decrease of C_{gd}/C_{gs} ratio (increase of $C_{channel}/C_{fringing}$ ratio), the increase of the fin numbers and thus the reduced values of the access resistances. Based on these simulation results, the reduction of the fin spacing appears to be a major technological issue for the next MuGFET generations for achieving high integration density level as well as high analog/RF performance.

We have presented simulation results of channel and fringing capacitances, comparing MuGFETs with SG, considering the same occupied die area. In order to optimize the RF performance of MuGFETs, their geometry has to fulfill the following design rules:

- fin spacing should be reduced down to 50 nm;
- SEG thickness should be kept between 30-50 nm for a good trade-off between low S/D resistances and parasitic capacitance;
- spacer thickness should be kept between 15-30 nm for a good trade-off as well;
- Pi-gate devices (referred gate extension depth of 10 nm) have a better $C_{channel}/C_{fringing}$ ratio than FinFETs and are, then, of interest for analog/RF applications.

Simulation of intrinsic capacitances related to DG MOSFET architectures in the presence of Volume Inversion

This part studies the effect of the volume inversion (VI) on the capacitances of undoped Double-Gate (DG) MOSFETs. For that purpose, we present simulation results for the capacitances of undoped DG MOSFETs using an explicit and analytical compact model. The model shows an accurate dependence on the silicon layer thickness, consistent with two dimensional numerical simulations, for both thin and thick silicon films. It demonstrates that the transition from volume inversion regime to dual gate behaviour is well simulated. Whereas the current drive and transconductance are enhanced in volume inversion regime, our results show that intrinsic capacitances present higher values as well, which may limit the high speed (delay time) behaviour of DG MOSFETs under volume inversion regime.
We demonstrate in this work that even for a silicon thickness of 40 nm we can observe evidence of VI. For this, we make comparisons between intrinsic capacitance values in a device with a very thick silicon film of 100 nm (where we do not expect VI) and for T_{Si} equal to 10 and 40 nm.
In this work, we do not consider quantum effects, since they can be assumed to be negligible for T_{Si} larger than 10 nm.
An undoped device is considered, with channel length L = 1 µm, a width of W = 1 µm, a silicon oxide thickness t_{ox} = 2 nm. We show the continuity of our model in the capacitance characteristics from subthreshold to strong inversion and from linear to saturation for different values of T_{Si}.
The capacitance C_{GS} presents a higher value (thus a higher I_{DS} value) for T_{Si} equal to 10 and 40 nm than for the case of T_{Si} = 100 nm, in weak inversion, for different V_{DS} values. This capacitance increase is directly related to an increase of the free carriers controlled by both gates under VI regime. It is worth noting that higher normalized capacitance C_{GS} values are already obtained for T_{Si} = 40 nm, which indicates that an efficient VI appears even for such silicon film thickness. For simplicity, a constant mobility value has been used in the DESSIS-ISE simulations and in our analytical model.
C_{GD} decreases in saturation with the reduction of the silicon film thickness, thanks to the better control of the channel carriers (due to a better electrostatic control short channel effects are diminished). We can see that our model predicts very well this behavior in the three cases considered: T_{Si}= 10, 40 and 100 nm. For a thinner silicon film we have a higher C_{GS}/C_{GD} ratio and so higher current gain and maximum available gain cutoff frequencies (f_T and *fmax*) which are of most importance in the RF domain [13].
In weak inversion, when V_{DS} = 1 V, for T_{Si} = 10 and 40 nm C_{GS} is higher than for T_{Si} = 100 nm. C_{GS} has the main contribution in saturation to C_{GG}, due to the fact that C_{GD} decreases with the reduction of the silicon film thickness. So we can safely assume that C_{GG} in weak inversion, for V_{DS} = 1 V, when T_{Si} = 10 and 40 nm is higher than C_{GG} when T_{Si} = 100 nm. Thus, in VI regime, besides the drain current (I_{DS}) increase related to the higher carrier mobility at the centre of the channel, we also see a total gate capacitance increase. Therefore, the decrease of the delay time with thinner T_{Si} for which VI regime is reached (for T_{Si} = 10 or 40 nm in our study) may not be as good as expected. Furthermore, if we dramatically decrease the silicon film thickness the mobility (and therefore the drain current) may decrease due to higher surface roughness scattering, and this would lead to a further increase of the delay time.

The model predicts well the dependence of capacitances with the reduction of the silicon layer thickness. The developed model simulates the volume inversion and Si film dependence thickness effects in the DG-MOSFET down to a silicon layer of 10 nm-thick.
Based on our results we have also analyzed the importance of volume inversion and its impact on RF and high speed factors of merit. We have concluded that the reduction of the Si film thickness in conditions of volume inversion, although of course it reduces short channel effects permitting the downscaling of the device's channel length, will not bring the expected improvement in terms of the delay time.

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